

CLAIM LISTING

1. (Currently Amended) A method of designing a logic circuit to provide a predetermined logical operation, the method including the steps of:
  - (a) defining a logic synthesis block comprising a single dynamic logic circuit;
  - (b) performing logic synthesis for the predetermined logical operation to produce an intermediate circuit, the logic synthesis being performed utilizing a synthesis library constrained to the logic synthesis block;
  - (c) eliminating unused devices in the intermediate circuit to produce a final circuit;
  - and
  - (d) sizing the devices in the final circuit.
2. (Original) The method of Claim 1 wherein the step of defining the logic synthesis block includes selecting the largest practical dynamic AND/OR circuit for the integrated circuit fabrication technology in which the circuit is to be implemented.
3. (Original) The method of Claim 2 wherein the logic synthesis block comprises a four high and four wide dynamic AND/OR circuit.
4. (Original) The method of Claim 1 wherein the step of performing logic synthesis includes leaving the size of the devices in the logic synthesis block substantially unconstrained.

1 5. (Original) The method of Claim 1 wherein the step of eliminating unused devices from  
2 the intermediate circuit includes detecting devices having a state that remains constant as  
3 the intermediate circuit operates to provide the predetermined logical operation.

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5 6. (Original) The method of Claim 1 wherein the step of sizing the devices in the final  
6 circuit includes analyzing the final circuit to determine the characteristics of each device  
7 in the final circuit necessary in order to consistently provide the predetermined logical  
8 operation and meet drive requirements.

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10 7. (Original) The method of Claim 1 wherein the logic synthesis block uses a single  
11 activation/reset clock signal.

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13 8. (Currently Amended) A method of synthesizing a logic circuit to provide a  
14 predetermined logical operation, the method including the steps of:  
15 (a) defining a logic synthesis block comprising a single dynamic logic circuit; and  
16 (b) performing logic synthesis for the predetermined logical operation to produce an  
17 intermediate circuit, the logic synthesis utilizing a synthesis library constrained to  
18 the single dynamic logic circuit comprising the logic synthesis block.

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20 9. (Original) The method of Claim 8 wherein the step of defining the logic synthesis block  
21 includes selecting the largest practical dynamic AND/OR circuit for the fabrication  
22 technology in which the circuit for performing the predetermined logical operation is to  
23 be implemented.

- 1 10. (Original) The method of Claim 8 wherein the logic synthesis block comprises a four  
2 high and four wide dynamic AND/OR circuit.  
3
- 4 11. (Original) The method of Claim 8 wherein the step of performing logic synthesis for the  
5 predetermined logical operation includes leaving device size in the logic synthesis block  
6 substantially unconstrained.  
7
- 8 12. (Original) The method of Claim 8 wherein the dynamic logic circuit comprising the logic  
9 synthesis block operates using a single activation/reset clock signal.  
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- 11 13. (Currently Amended) In a circuit design method utilizing a logic synthesis tool and  
12 predefined logic circuit library to provide a logic implementation for a predetermined  
13 logical operation, the improvement comprising:  
14 (a) defining a logic synthesis block comprising a single dynamic logic circuit; and  
15 (b) constraining the logic synthesis tool to the logic synthesis block.  
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- 17 14. (Original) The method of Claim 13 wherein the logic synthesis tool produces an  
18 intermediate circuit design which performs the predetermined logical operation, and  
19 further including the steps of:  
20 (a) eliminating unused devices in the intermediate circuit design to produce a final  
21 circuit; and  
22 (b) sizing the devices in the final circuit.  
23

1 15. (Original) The method of Claim 13 wherein the step of defining the logic synthesis block  
2 includes selecting the largest practical dynamic AND/OR circuit for the circuit fabrication  
3 technology in which the circuit design is to be implemented.

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5 16. (Original) The method of Claim 13 wherein the logic synthesis block comprises a four  
6 high and four wide dynamic AND/OR circuit.

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8 17. (Original) The method of Claim 13 further including the step of leaving the device size  
9 in the logic synthesis block substantially unconstrained for the logic synthesis tool.

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11 18. (Original) The method of Claim 13 wherein the logic synthesis block uses a single  
12 activation/reset clock input.